

Claims

1 1. A method of forming an isolation in a semiconductor substrate comprising:
2 (a) providing a semiconductor substrate;
3 (b) forming a plurality of adjacent trenches in said semiconductor substrate
4 leaving adjacent segments of said semiconductor substrate between each of
5 said adjacent trenches;
6 (c) depositing a barrier layer in said plurality of adjacent trenches;
7 (d) removing a portion of said barrier layer in each of said plurality of adjacent
8 trenches to expose portions of said adjacent segments of said semiconductor
9 substrate,
10 (e) merging said exposed portions of said adjacent segments of said
11 semiconductor substrate to form a self-aligned shallow trench isolation.

1 2. The method of claim 1 wherein step (a) comprises providing a silicon substrate
2 having a pad dielectric layer thereover a surface of said silicon substrate.

1 3. The method of claim 2 wherein said pad dielectric layer comprises a pad oxide
2 layer followed by a pad nitride layer.

1 4. The method of claim 1 wherein step (b) comprises etching a plurality of
2 adjacent vertical deep trenches in said semiconductor substrate leaving said adjacent
3 segments of said semiconductor substrate between each of said plurality of adjacent
4 vertical deep trenches.

1 5. The method of claim 1 wherein step (c) comprises depositing an oxidation
2 barrier layer in said plurality of adjacent trenches.

1 6. The method of claim 1 wherein step (e) comprises merging said exposed
2 portions of said adjacent segments of said semiconductor substrate by oxidation to
3 form a self-aligned thermal oxide shallow trench isolation.

1 7. The method of claim 1 further including after step (e) the steps comprising:
2 (f) removing remaining portions of said barrier layer in said plurality of adjacent
3 trenches;
4 (g) forming a deep trench capacitor within said plurality of adjacent trenches; and
5 (h) forming a vertical transistor within said plurality of adjacent trenches to form
6 a memory cell.

1 8. A method of forming isolations in a semiconductor substrate comprising:
2 (a) providing a silicon substrate;
3 (b) forming a plurality of adjacent trenches leaving adjacent segments of said
4 silicon substrate between each of said plurality of adjacent trenches;
5 (c) depositing an oxidation barrier layer in said plurality of adjacent trenches;
6 (d) recessing a portion of said oxidation barrier layer in each of said plurality of
7 adjacent trenches to expose at least a portion of said adjacent segments of said
8 silicon substrate;
9 (e) etching said exposed portions of said adjacent segments of said silicon
10 substrate to form a plurality of thin sections of said exposed adjacent segments
11 of said silicon substrate between each of said plurality of adjacent trenches;
12 and
13 (f) merging said thin sections of said exposed adjacent segments of said silicon
14 substrate at least along a first row of selected ones of said plurality of
15 adjacent trenches to form a self-aligned shallow trench isolation.

- 1 9. The method of claim 8 wherein step (a) further comprises depositing a layer of
2 pad oxide thereover said silicon substrate to a thickness ranging from about 1 to about
3 10 nm.
- 1 10. The method of claim 9 wherein step (a) further comprises depositing a layer of
2 pad nitride thereover said layer of pad oxide to a thickness ranging from about 50 to
3 about 500 nm.
- 1 11. The method of claim 8 wherein step (b) comprises etching said plurality of
2 adjacent trenches to a depth ranging from about 250 nm to about 10 μ m.
- 1 12. The method of claim 8 wherein step (c) comprises depositing said oxidation
2 barrier layer to at least conformally coat a sidewall and a bottom surface of said
3 plurality of adjacent trenches.
- 1 13. The method of claim 8 wherein step (c) comprises depositing an oxidation
2 barrier layer of silicon nitride having a thickness ranging from about 3nm to about
3 30nm.
- 1 14. The method of claim 8 wherein said step (d) of recessing said portion of said
2 oxidation barrier layer comprises:
3 depositing a photoresist within said plurality of adjacent trenches to at least fill
4 empty portions of said plurality of adjacent trenches;
5 determining a desired depth in said photoresist to recess said oxidation barrier
6 layer;
7 etching said photoresist and said oxidation barrier layer stopping at said desired
8 depth in said photoresist thereby recessing said oxidation barrier layer to said

9 desired depth and exposing said portions of said adjacent segments of silicon
10 substrate in a top portion of said plurality of adjacent trenches.

1 15. The method of claim 12 wherein step (d) comprises recessing said oxidation
2 barrier layer to a depth ranging from about 20nm to about 2000nm within said
3 plurality of adjacent trenches.
4 recessing a portion of said oxidation barrier layer in each of said plurality of adjacent
5 trenches to expose at least a portion of said adjacent segments of said silicon
6 substrate.

1 16. The method of claim 8 wherein step (e) said etched plurality of thin sections
2 of said exposed adjacent segments of said silicon substrate have a diameter ranging
3 from about 1/5 to about 1/2 that of an original diameter of said exposed portions of
4 said adjacent segments of said silicon substrate.

1 17. The method of claim 8 wherein step (e) comprises etching said exposed
2 portions of said adjacent segments of said silicon substrate using an etchant which
3 selectively removes only said silicon substrate to form said plurality of thin sections of
4 said exposed adjacent segments of said silicon substrate.

1 18. The method of claim 17 wherein said etchant comprises an etchant selected
2 from the group consisting of a chlorine-containing etchant, KOH, and NH₄OH.

1 19. The method of claim 8 wherein step (f) comprises oxidizing said thin sections
2 of said exposed adjacent segments of said silicon substrate thereby merging together
3 selected ones of said thin sections of adjacent segments of said silicon substrate at
4 least along said first row of said selected ones of said plurality of adjacent trenches to
5 form a self-aligned silicon dioxide shallow trench isolation.

1 20. The method of claim 19 wherein said thin sections of said exposed adjacent
2 segments of said silicon substrate are oxidized using a local oxidation of silicon.

1 21. An isolation structure in a semiconductor substrate comprising:
2 a semiconductor substrate;
3 a plurality of adjacent trenches in said semiconductor substrate; and
4 a self-aligned isolation structure in upper portions of selected ones of said
5 plurality of trenches, said isolation structure being merged portions of said
6 semiconductor substrate along at least a first row of said selected ones of
7 said plurality of adjacent trenches, said merged portions of said
8 semiconductor substrate being aligned as-formed to edges of said plurality of
9 adjacent trenches,
10 wherein said self-aligned isolation structure isolates a first region of said
11 semiconductor substrate from a second region of said semiconductor substrate.

1 22. The apparatus of claim 21 wherein said semiconductor substrate comprises a
2 silicon substrate.

1 23. The apparatus of claim 21 further including a pad dielectric layer thereover a
2 surface of said semiconductor substrate.

1 24. The apparatus of claim 23 wherein said pad dielectric layer comprises a pad
2 oxide layer followed by a pad nitride layer.

1 25. The apparatus of claim 24 wherein said pad oxide layer has a thickness
2 ranging from about 1 nm to about 10 nm.

1 26. The apparatus of claim 24 wherein said pad nitride layer has a thickness
2 ranging from about 50 nm to about 500 nm.

1 27. The apparatus of claim 21 wherein said plurality of adjacent trenches have
2 depths ranging from about 250 nm to about 10 μ m.

1 28. The apparatus of claim 21 wherein said self-aligned isolation structure
2 comprises a thermal oxide region existing along said at least first row of selected ones
3 of said plurality of adjacent trenches.

1 29. The apparatus of claim 28 wherein said semiconductor substrate comprises a
2 silicon substrate and said thermal oxide region comprises a thermal silicon dioxide
3 region existing along said at least first row of selected ones of said plurality of
4 adjacent trenches.

1 30. An isolation structure in a semiconductor substrate comprising:
2 a silicon substrate having a layer of pad oxide disposed thereover said silicon
3 substrate and a layer of pad nitride disposed thereover said pad oxide;
4 a plurality of adjacent trenches traversing through said pad oxide, said pad
5 nitride, and stopping in said silicon substrate; and
6 a self-aligned, thermal oxide isolation structure in upper portions of said
7 plurality of adjacent trenches, said thermal oxide isolation structure being
8 oxidized portions of said semiconductor substrate merged along at least a
9 first row of selected ones of said plurality of adjacent trenches in said upper
10 portions of said trenches, said oxidized portions of said semiconductor
11 substrate being aligned as-formed to edges of said plurality of adjacent
12 trenches,

13 wherein said thermal oxide isolation structure isolates a first region of said
14 semiconductor substrate from a second region of said semiconductor substrate.